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A PARYLENE COATING PROCESS FOR HYBRID CIRCUITS

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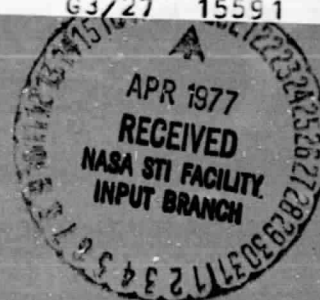
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ABSTRACT

Development of Parylene Coating Process for Hybrid Circuits

Application of parylene for protecting microelectronic circuits from loose particles and external environment has been visualized for many years. With a joint effort by NASA and TMD, a process has now been qualified to perform parylene deposition on hybrid circuits on a production basis.

The parylene coating process developed during this program consists of a) obtaining a hybrid cover with a hole in it, b) sealing of the circuit with a hole in the cover, c) parylene coating through the hole with the external leads protected from parylene by appropriate fixturing, and d) sealing of the hole by soldering a pretinned kovar tab. Development of the above process required optimization of the parylene coater parameters to obtain a uniform consistent coating which could offer adequate protection to the circuits, fixture design for packages of various types, determination of the size of the deposition hole, and the amount of dimer charge per run, a process to hermetically seal the deposition holes and establishment of quality control techniques or acceptance criteria for the deposited film.

Several experimental runs were made on test circuits as well as actual production circuits to determine the effect of parylene coating on active components, thin film resistors, and wire bonds under various conditions. Tests were also made to determine if parylene indeed protected circuits from loose particles and external environment.

After these experiments, parylene coating acceptance standards were established and a long and rigorous qualification program was completed in order to prove the feasibility of this process. The results of the qualification program will be reported in a future publication.

It is concluded that parylene offers excellent protection against loose particles and a degree of protection from some environmental conditions. It is expected that the fraction of hybrids being coated with parylene will continue to increase in the microelectronic industry.

INTRODUCTION

Parylenes* belong to a family of linear plastic polymers. The basic member of this family, called Parylene N, is polyparaxylene. Parylenes are known to be extremely crystalline straight chain compounds with good dielectric strength, high surface and volume resistivities, excellent tensile strength, and extremely good resistance to chemical attack (See Reference 1). Additionally, parylenes can be vacuum deposited in the form of thin films with unusually high penetration power which can act as protective barriers against mechanical and chemical attack. Parylene C, or polymonochloroxylene, the polymer chosen for this investigation, has been used as a passivation in electronic circuitry for a number of years. In fact, its application in microelectronics has been conceived and studied for some time (See Reference 2 and 3). The real impetus for developing a production parylene coating process for internal hybrid passivation came as a result of the possibility of loose conductive particles in hybrid microelectronic circuits, causing intermittent and sometimes permanent failures, especially in space applications. Because of the excellent mechanical properties of parylene, it is capable of securing the loose particles in place and preventing such failures. Particles on top of parylene cannot create shorts because of its insulation properties. After considerable developmental work at TM with NASA/LeRC support in the areas of tooling, coating process parameters, hermetic sealing of finished hybrid packages, and process control techniques, internal parylene coating has now become a viable production process. NASA/Centaur hybrids are being coated with parylene at TM at the present time.

The process of coating consists of:

1. Vaporizing the initial charge, which is in the form of a dimer,
2. Conversion of the dimer into a reactive monomer, and
3. Deposition and subsequent polymerization of the monomer in the deposition chamber which forms a uniform Parylene film over all the cold surfaces it contacts.

*Registered Trademark of Union Carbide Corporation

INTRODUCTION (CONTINUED)

Parylene process flow and the individual chemical reactions are shown in Figure 1. Typical properties of various parylenes are listed in Table 1. (See Reference 4.)

Table 1. Typical Properties of Various Parylenes

	Parylene N	Parylene C	Parylene D
Dielectric Strength. Short time Volts/Mil at 1 Mil	7000	5600	5500
Volume resistivity 23°C 50% RH ohm cm	1×10^{17}	6×10^{16}	2×10^{16}
Dielectric Constant			
60 Hz	2.65	3.15	2.84
10^3 Hz	2.65	3.10	2.82
10^6 Hz	2.65	2.95	2.80
Melting or heat distortion temperature	405	280	>350
Tensile strength PSI	6500	10,000	11,000
Elongation to Break Per- cent	30	200	10
Yield strength PSI	6100	8000	9000
Yield Elongation Percent	2.5	2.9	3.0
Moisture Vapor Transmission g/mil/100 in 24 hours 37°C - 90 percent RH	1.6	0.5	0.25
Linear thermal coefficient of expansion ($10^{-5}/^{\circ}\text{C}$)	6.9	3.5	---

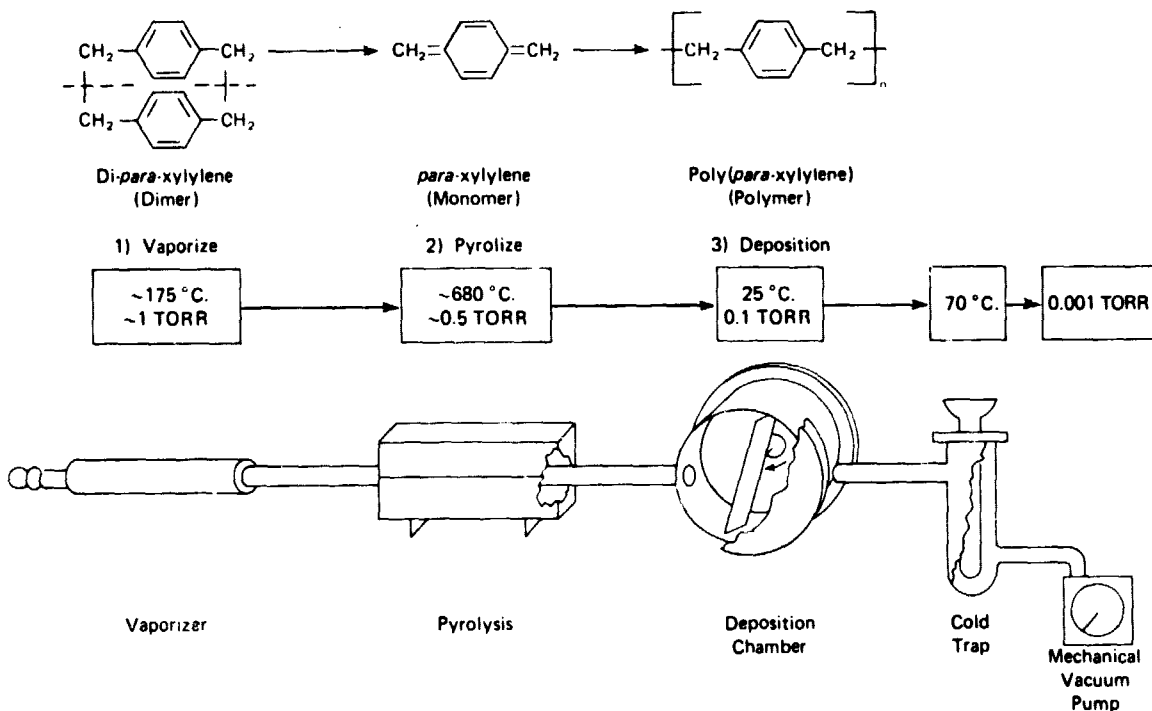


DIAGRAM OF THE PARYLENE PROCESS

Figure 1

Reproduced from Union Carbide Parylene Brochure, July 1974.

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INTRODUCTION (CONTINUED)

It should be noted that the monomer vapor has extremely high penetration power. Uniform coatings are obtained over edges, points, and internal areas. This is the secret of the ability of Parylene to passivate hybrid circuits with extremely thin films of the order of .0001" or less. Additionally, deposition in the vapor phase and freedom from straight line deposition effects makes it possible to perform uniform Parylene coating through a hole in the hybrid cover. The development phase of this program is discussed in the following.

PROCESS DEVELOPMENT

Although high penetration power of the monomer vapor is advantageous in terms of achieving coating uniformity, it poses problems in other areas, namely the sealing surfaces and the leads. Parylene coats any surface to which access in a gaseous phase is possible. In other words, unless the surface to be protected is in an independent vacuum tight region, it will get a small amount of Parylene coating. Even small amounts make the surface unwettable by solder and also make electrical contact through the surface difficult to achieve. Initially, Parylene coating was attempted on open hybrids before cover seal, but that approach was soon abandoned because:

1. It became very difficult to protect the sealing surface from Parylene, and
2. Parylene always formed a film on the inner surface of the fixtures which could not be peeled off without damaging the part in some instances.

Subsequently, it was decided to use the hole in the cover approach to coat the parts. The details of the process development were as follows:

1. Tooling

This was the most important part of the development in terms of protecting external leads from Parylene. In less critical applications masking tapes and RTV silicone compounds have been effectively used to obtain the necessary protection, but in the case of many hybrids, the leads are rather fragile which means they have to be protected without causing undue stresses in them. Cavity plus gasket type fixtures were designed for various part types to achieve the requisite degree of protection. In order to load an optimum number of parts, it was decided that the fixtures would be in the form of blades which could be loaded onto the central rotor in the Parylene chamber. Parts could be loaded on both sides of the blades except in the case of TO-8 header type parts. Each blade consisted of a central plate with appropriate cavities on both sides for a particular package type. There were individual silicone rubber gaskets which were loaded on top of the package covers and main gaskets that covered the periphery of each side of the control plate. The top plates with holes for Parylene to

PROCESS DEVELOPMENT (CONTINUED)

1. Tooling (Continued)

enter were then loaded on either side and counter-sunk screws were used to tighten the whole assembly. The blades were then mounted on a carousel which was loaded onto the rotor in the center of the Parylene chamber. Figure 2 shows various parts of the fixture with appropriate packages loaded in some cavities as an example, and Figure 3 shows a completely loaded chamber.

2. Size of the Deposition Hole

The process of determining the optimum deposition hole size was conducted with test runs to find the effect of the hole size on the thickness of the internal coating. Generally, a smaller hole size was desirable to make the subsequent sealing of the deposition hole easier. A larger size on the other hand, would increase the thickness of the internal coating for a standard outside thickness. A smaller dimer charge could therefore be used to achieve the same internal thickness, thereby reducing the cost of the material and the total coating cycle time. A number of tests were run to study the effect of the hole size and the internal area of the package on the internal parylene thickness. Basically, three different hole sizes; namely, 22 mil dia, 31 mil dia, and 40 mil dia, were chosen. Package areas ranged from 0.1 square inch to 3.87 square inches. A standard outside coating thickness of 0.6 mils was used throughout this investigation. Internal thickness of parylene for the packages was determined by carefully weighing the packages before and after parylene coating. The results of these tests are plotted in Figure 4.

It is evident from these results that if a strict control on the inside parylene thickness is desired, it is necessary to control the package hole size and the external thickness of parylene. Additionally, it is not feasible to coat packages with a large difference in the internal areas at the same time unless the deposition hole sizes are chosen according to the internal areas of the package.

Earlier experiments had shown that even 60-80 microinches of parylene is sufficient to hold down loose particles. With the high breakdown voltage of Parylene, its exceptional

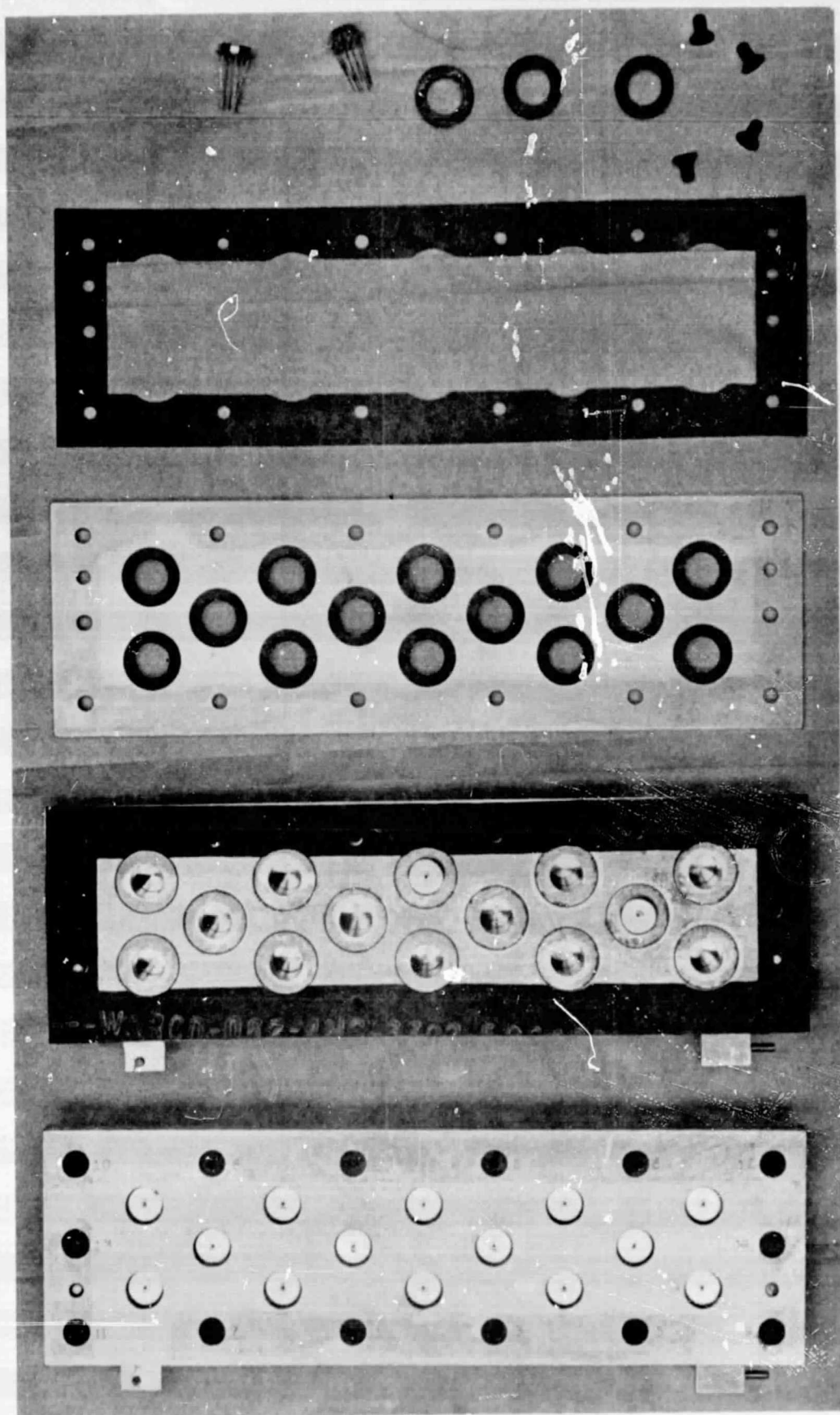


Figure 2. Various Parts of the Parylene Fixture Used For TO-8 Packages

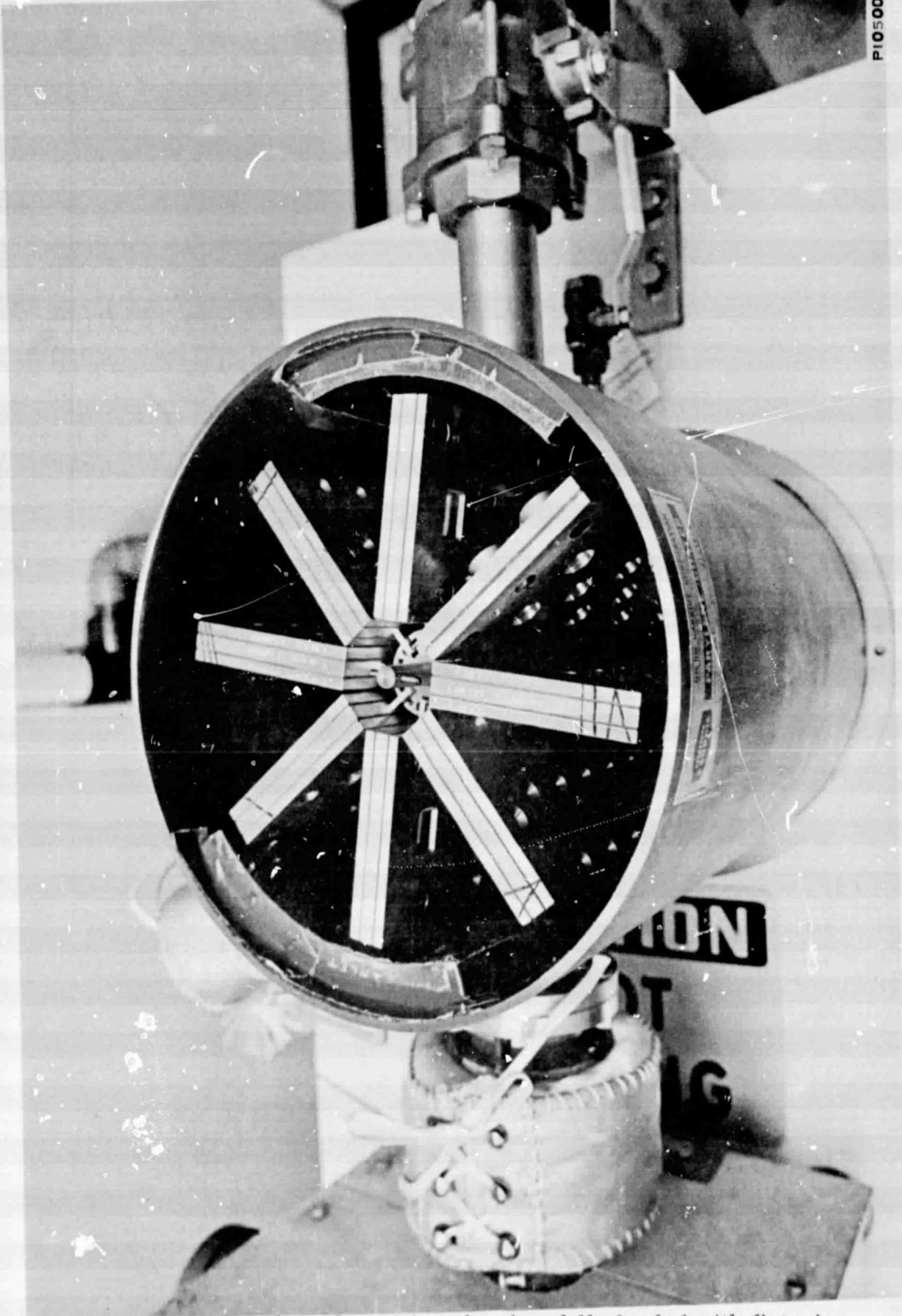


Figure 3. Parylene deposition chamber fully loaded with fixturing.

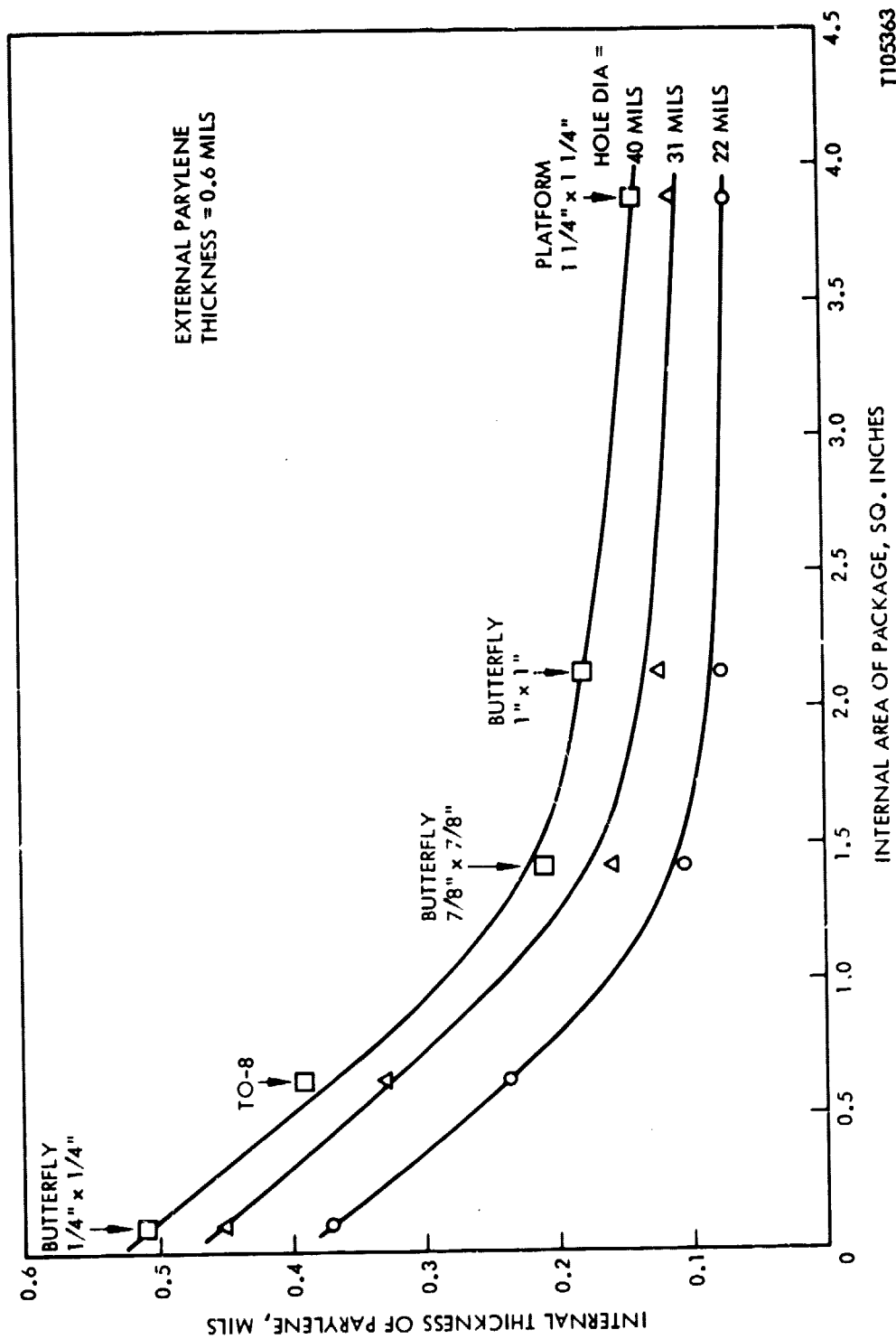


Figure 4. Internal Area Vs. Internal Parylene Thickness For Various Packages

PROCESS DEVELOPMENT (CONTINUED)

2. Size of the Deposition Hole (Continued)

mechanical properties and chemical resistance, it was decided that a minimum thickness of 0.1 mil would be satisfactory for NASA/TM purposes. Since the largest package used on the NASA/Centaur program had less than 1.5 square inches of internal area, it was determined that a final outside thickness of 0.6 mils and a hole diameter of 31 mils (1/32") would give an acceptable coating for packages smaller than 1.5 square inches in the internal area. Subsequent work in other areas did indicate that the choice of hole size was correct.

3. Parylene Coater Parameters

Initially several runs were made at settings recommended by Union Carbide. The most important coater parameters were known to be the vaporizer temperature and the pyrolyzer temperature. For hybrid applications, it was found that the maximum pressure change during the run was also an important control parameter to avoid coating non-uniformity within the hybrid packages. A number of runs were made on standard 1" x 3/4" packages with the Parylene coater parameters at different settings. Incidentally, these were the runs in which various experimental units were coated. These units were subsequently used for wire bond reliability tests, thin film resistor tests, and loose particle tests. The results of these experiments are discussed in a later section. The effect of the above parameters on the final Parylene film are listed in Table 2.

It can be seen that reasonable variations in the coater parameters still provide an acceptable product. It should be noted, however, that severely degraded vacuum during a run might pose problems if the situation remains uncorrected. Non-uniform coatings with globules of high dimer Parylene are obtained when the vapors are contaminated by oxygen. Additionally, the maximum pressure rise over base pressure is found to be important for maintaining film quality. Typical relationship between chamber pressure and elapsed time is shown in Figure 5.

Table 2

Effect of Various Parameters on Finished Parylene Film

Run No.	Control		Maximum Pressure Levels		Parylene Properties				Remarks
	Δ Vaporizer °C	Δ Furnace °C	Pump (Microns)	Δ Line (Microns)	Outside Thickness	Film Quality	Inside Thickness	Dimer Content	
1	-30	+35	1.0	-15	0.67	Good	0.13 0.14	0.66%	Low vaporizer high furnace run
2	0	-5	1.5	+2	0.67	Good	0.13 0.14	5.0%	High vaporizer low furnace run
3	-15	+15	1.5	+7	0.74	Good	0.13 0.15	1.21%	Degraded line vacuum run
4	-15	+15	0.5	-2	0.61	Good	0.125 0.13	1.19%	Standard run
5	-15	+15	5.7	+4	----	Good	0.14 0.14	0.89%	Degraded pump vacuum run
6	-10	+15	0.8	-2	0.62	Good	0.13 0.16	1.06	Standard run

NOTE: Δ Vaporizer Δ Pyrolyzer, Δ line are defined as the difference between the actual recorded value and that value suggested by Union Carbide in their proprietary letter.

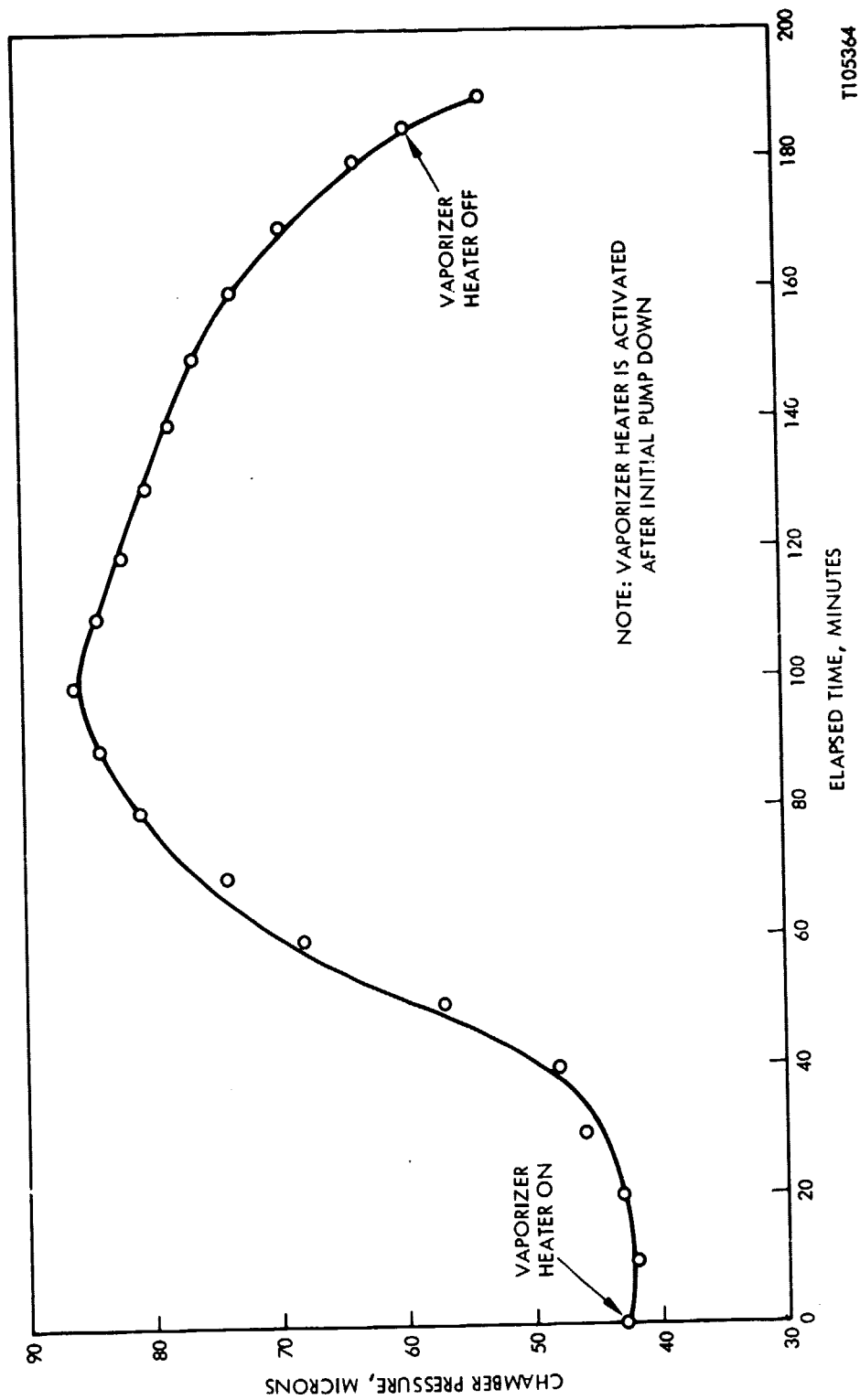


Figure 5. Typical Parylene Run Chamber Pressure Vs. Elapsed Time

PROCESS DEVELOPMENT (CONTINUED)

4. Secondary Control System

Early in the development of the Parylene coating process it was realized that certain coater parameters, namely, vaporizer temperature, furnace temperature, and line vacuum, had to be controlled within certain ranges to obtain a satisfactory product. Because of the potential cost of hardware going into each run, loss of a single run could prove disastrous. A backup control panel was therefore installed to:

- (a) Continuously monitor the above parameters and indicate undue deviations, and
- (b) Enable the operator to control any of the above parameters with the help of the backup control system in case of a failure of the primary controls. Although none of the primary controls has failed so far, there is always the possibility that the secondary control system might be pressed into service to save a few runs in the future.

5. Hermetic Sealing of the Deposition Hole

Hermetic sealing of the hole is accomplished by using a solder plated disc shaped Kovar tab which is slightly larger than the hole itself. Essentially, the tab is placed over the gold plated cover and the solder reflowed with a pulse type soldering iron which has an automatic timer with a manual cutoff switch connected to a foot pedal. When the solder is seen to melt and flow on the gold plating on the cover, the iron is turned off. The solder is allowed to freeze and then the iron is removed from the tab. The whole operation takes place in an inert atmosphere. Production experience has shown that satisfactory yields have been obtained in this process since its inception. Typical device in various stages of hole sealing is shown in Figure 6.

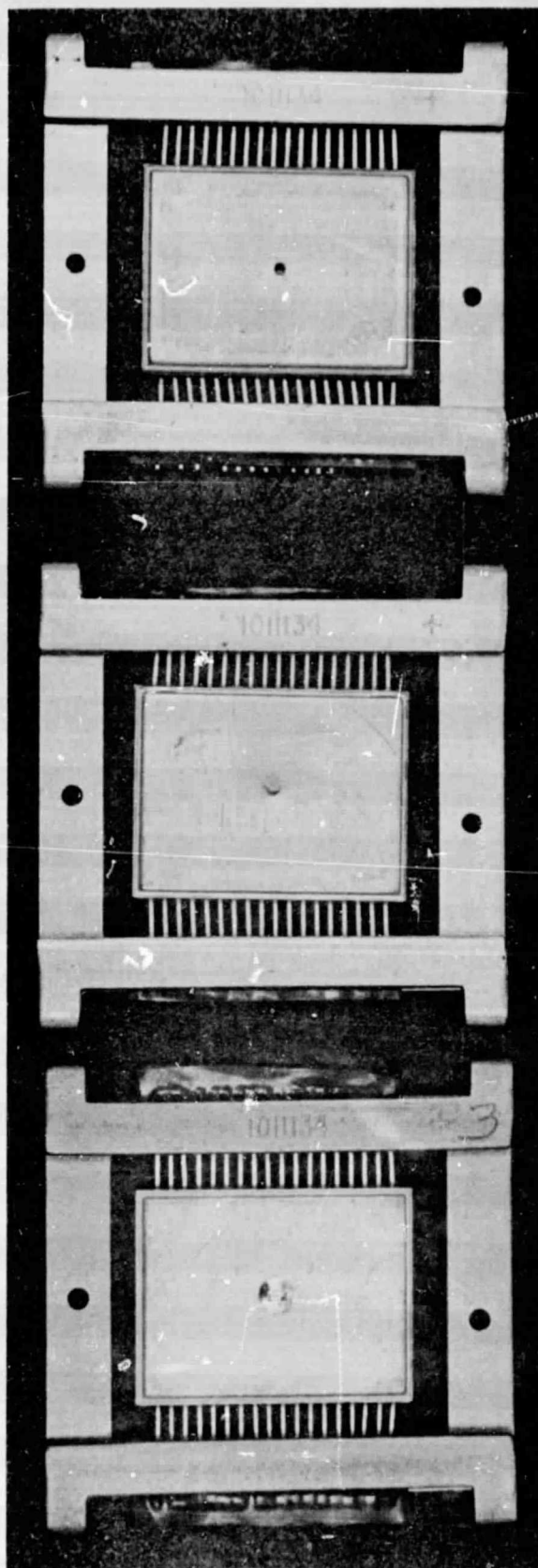


Figure 6. Typical Device in Various Stages of Hole Sealing Operation

EXPERIMENTAL RESULTS

1. Wire Bond Reliability

Since Parylene has a thermal expansion coefficient that is large compared to other materials in a hybrid, it was feared that temperature changes could cause wire bond failures. Thermal cycling of Parylene coated .001" aluminum wire bonds was thought to be the best test to study the effects of Parylene on bonds.

The first test undertaken to study wire bond integrity consisted of five (5) Parylene coated bond test patterns with 400 bonds each, and five (5) control units with the same number of bonds. These test patterns were specially designed and bonded to determine bond integrity through an electrical continuity check. After an initial check to assure that all the bonds were intact, the units were subjected to continuous thermal cycling from -55°C to $+125^{\circ}\text{C}$, with continuity checks at frequent intervals. The experiment was terminated with a final check at 1000 cycles. The results of this test yielded no bond failures in Parylene coated units, whereas one bond failed on one of the control units at 750 cycles. It should be noted that the Parylene coated group in this case had between 0.5 to 0.6 mils of coating. If any detrimental effects on lead bonds due to the difference in thermal expansion coefficient or other phenomena are possible, they should have been apparent in this investigation. No such effects were noted.

The second test consisted of a total of twelve (12) bond test patterns bonded with .001" diameter aluminum wire. Two of the test patterns were left as controls and the other ten (10) were Parylene coated through a hole in the cover in five different runs, with the Parylene process control parameters set at different levels (See Table 2). The parts were then thermal cycled continuously from -55°C to $+125^{\circ}\text{C}$ with pull tests of 10 bonds from each package at frequent intervals. The results of this test are presented in Table 3.

Table 3. Average Bond Pull Strength
During Thermal Cycling
(Grams)

Run No.	After Parylene	130 Cycles	380 Cycles	630 Cycles	880 Cycles	1000 Cycles
1	6.8	7.3	8.1	6.7	6.3	6.5
2	7.5	7.8	8.0	7.7	6.5	6.8
3	6.6	8.0	7.8	7.0	5.6	5.9
4	7.8	7.6	8.1	7.6	6.6	6.8
5	8.0	7.7	7.2	7.5	6.4	6.2
Controls	6.0	5.5	5.5	4.2	4.7	4.5

1. Wire Bond Reliability (Continued)

It can be seen that no harmful effects on wire bond integrity are observed due to Parylene coating.

2. Resistor Drift

Two experiments were performed to study thin film resistor drift. In the first experiment ten (10) resistor networks were wire bonded to test 12 resistors on each network. After standard screens consisting of 24 hours at 150°C and 10 thermal cycles at -65°C to +150°C, all the resistors went through the following operations:

- (a) Initial measurements
- (b) Parylene coating in five separate runs with two resistor networks per run.
- (c) Second resistance measurements
- (d) Simulated burn-in at 100°C for 168 hours

EXPERIMENTAL RESULTS (CONTINUED)

2. Resistor Drift (Continued)

- (e) Third resistance measurement
- (f) Second simulated burn-in at 100°C for 168 hours
- (g) Final resistance measurements

The results of this experiment are described in Table 4. It is noted that the percent changes in resistance are cumulative.

Table 4. Effect of 100°C Burn-In on Thin Film
Resistors Coated with Parylene

Parylene Run No.	Maximum Percent Change in Resistance		
	Parylene Coating	First Burn-In	Second Burn-In
1	Not Detectable	.009%	.017%
2	Not Detectable	.009%	.018%
3	Not Detectable	.009%	.014%
4	Not Detectable	.008%	.013%
5	Not Detectable	.009%	.015%

In the other experiment, fifteen 50K ohm/100K ohm 12 bit ladder networks were bonded to measure 12 resistors on each network. After 48 hours of heat soak at 150°C and 85% humidity treatment at 75°C for 24 hours, the parts were divided into two groups. The first group, consisting of five (5) units, was left as control. The other group of ten (10) was subjected to Parylene coating in five separate runs. After coating and initial resistance measurements, all the units underwent thermal cycling from -55°C to +125°C

EXPERIMENTAL RESULTS (CONTINUED)

2. Resistor Drift (Continued)

for 60 complete cycles with 22 volts applied to each resistor. These units were not cover sealed because the intent of the test was to study possible degradation of nichrome resistors due to electrolytic action in humid atmosphere. After thermal cycling final resistance measurements were taken to complete the test.

All 120 Parylene coated resistors showed nominal changes (.03% max) after thermal cycling, whereas in the uncoated control group, 3 resistors opened up due to electrolytic action and two more resistors registered drastic changes. The total control sample consisted of 60 resistors.

From this test data it can be concluded that Parylene does not have a damaging effect on the resistors. On the other hand, electrolytic degradation of resistors caused by the presence of moisture and electric field may be prevented by the protective film of Parylene.

Controlled experiments were performed on electrically operative units with various types of loose particles purposely introduced into them before and after Parylene coating. Parylene offered protection against the loose particles in every case. A long and rigorous Parylene qualification program was also completed at TM with excellent results. The advantages of Parylene coating have been well verified to date. The details of these experiments will be included in a future publication.

COATING ACCEPTANCE STANDARDS

After every run the dimer content and the thickness of the finished Parylene film in test units are checked by the Quality Control organization. If the above two properties are within acceptable limits and the finished Parylene film passes visual examination, the run is considered acceptable.

CONCLUSION

It is concluded that internal cavities of all types of microelectronic circuits can be successfully coated with Parylene provided appropriate tooling is utilized to protect external leads from the Parylene monomer. Tests show that Parylene deposited under controlled conditions provides good protection against intermittent failures due to loose conductive particles. It also appears to act as a barrier against thin film resistor failures due to electrolytic action.

A large number of production runs have been made at TM after the completion of the qualification program. Performance of the production units has shown no adverse effects attributable to Parylene. With the degree of success achieved to date, it can be expected that the fraction of hybrids being Parylene-coated will be on an increase in the microelectronic industry within the imminent future.

Further information may be had by contacting:

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